1-Wire Bus System

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances the DS1922E is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master.

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS1922E is open drain with an internal circuit equivalent to that shown in Figure 10.

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. At standard speed the 1-Wire bus has a maximum data rate of 16.3kbps. The speed can be boosted to 142kbps by activating the Overdrive Mode. The DS1922E is not guaranteed to be fully compliant to the iButton device standard. Its maximum data rate in standard speed is 15.4kbps and 125kbps in overdrive speed. The value of the pullup resistor primarily depends on the network size and load conditions. The DS1922E requires a pullup resistor of maximum 2.2kΩ at any speed.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus **must** be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16µs (overdrive speed) or more than 120µs (standard speed), one or more devices on the bus may be reset. Note that the DS1922E does not quite meet the full 16µs maximum low time of the normal 1-Wire bus overdrive timing. With the DS1922E the bus must be left low for no longer than 12µs at overdrive to ensure that no DS1922E on the 1-Wire bus performs a reset. The DS1922E communicates properly when used in conjunction with a DS2480B or DS2490 1-Wire driver and adapters that are based on these driver chips.

Transaction Sequence

The protocol for accessing the DS1922E through the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory/Control Function Command
- Transaction/Data

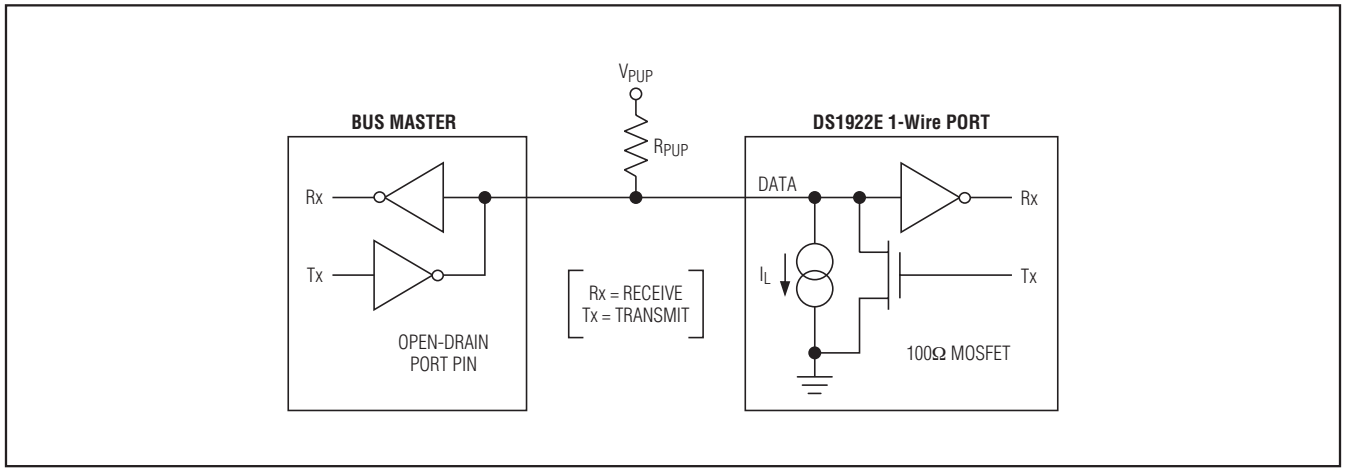


Figure 10. Hardware Configuration

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS1922E is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

1-Wire ROM Function Commands

Once the bus master has detected a presence, it can issue one of the eight ROM function commands that the DS1922E supports. All ROM function commands are 8 bits long. A list of these commands follows (see the flowchart in Figure 11).

Read ROM [33h]

This command allows the bus master to read the DS1922E's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number results in a mismatch of the CRC.

Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS1922E on a multidrop bus. Only the DS1922E that exactly matches the 64-bit ROM sequence responds to the following memory function command. All other slaves wait for a reset pulse. This command can be used with a single device or multiple devices on the bus.

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their registration numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the registration numbers of all slave devices. For each bit of the registration number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its registration number bit. On the second slot, each slave device participating in the search outputs the complemented value of its registration number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the ROM code tree. After one complete pass, the bus master knows the registration number of a single device. Additional passes identify the registration numbers of the remaining devices. Refer to Application Note 187: *1-Wire Search Algorithm* for a detailed discussion, including an example.

Conditional Search ROM [ECh]

The Conditional Search ROM command operates similarly to the Search ROM command except that only those devices that fulfill certain conditions participate in the search. This function provides an efficient means for the bus master to identify devices on a multidrop system that have to signal an important event. After each pass of the conditional search that successfully determined the 64-bit ROM code for a specific device on the multidrop bus, that particular device can be individually accessed as if a Match ROM had been issued, since all other devices have dropped out of the search process and are waiting for a reset pulse.

The DS1922E responds to the Conditional Search ROM command if one of the three alarm flags of the Alarm Status register (address 0214h) reads 1. The temperature alarm only occurs if enabled (see the *Temperature Sensor Alarm* section). The BOR alarm is always enabled. The first alarm that occurs makes the device respond to the Conditional Search ROM command.

Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. For example, if more than one slave is present on the bus and a Read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Resume [A5h]

The DS1922E must be accessed several times before a mission starts. In a multidrop environment this means that the 64-bit ROM code after a Match ROM command must be repeated for every access. To maximize the data throughput in a multidrop environment, the Resume function was implemented. This function checks the status of the RC bit and, if it is set, directly transfers control to the memory/control functions, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM, Search ROM, or Overdrive-Match ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume command function. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume command function.

Overdrive-Skip ROM [3Ch]

On a single-drop bus this command can save time by allowing the bus master to access the memory/control functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command, the Overdrive-Skip ROM command sets the DS1922E in the Overdrive Mode (OD = 1). All communication following this command must occur at overdrive speed until a reset pulse of minimum 690µs duration resets all devices on the bus to standard speed (OD = 0).

When issued on a multidrop bus, this command sets all overdrive-supporting devices into Overdrive Mode. To subsequently address a specific overdrive-supporting device, a reset pulse at overdrive speed must be issued followed by a Match ROM or Search ROM command sequence. This speeds up the time for the search process. If more than one slave supporting overdrive is present on the bus and the Overdrive-Skip ROM command is followed by a Read command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Overdrive-Match ROM [69h]

The Overdrive-Match ROM command followed by a 64-bit ROM sequence transmitted at overdrive speed allows the bus master to address a specific DS1922E on a multidrop bus and to simultaneously set it in Overdrive Mode. Only the DS1922E that exactly matches the 64-bit ROM sequence responds to the subsequent memory/control function command. Slaves already in Overdrive Mode from a previous Overdrive-Skip ROM or successful Overdrive-Match ROM command remain in Overdrive Mode. All overdrive-capable slaves return to standard speed at the next reset pulse of minimum 690µs duration. The Overdrive-Match ROM command can be used with a single or multiple devices on the bus.

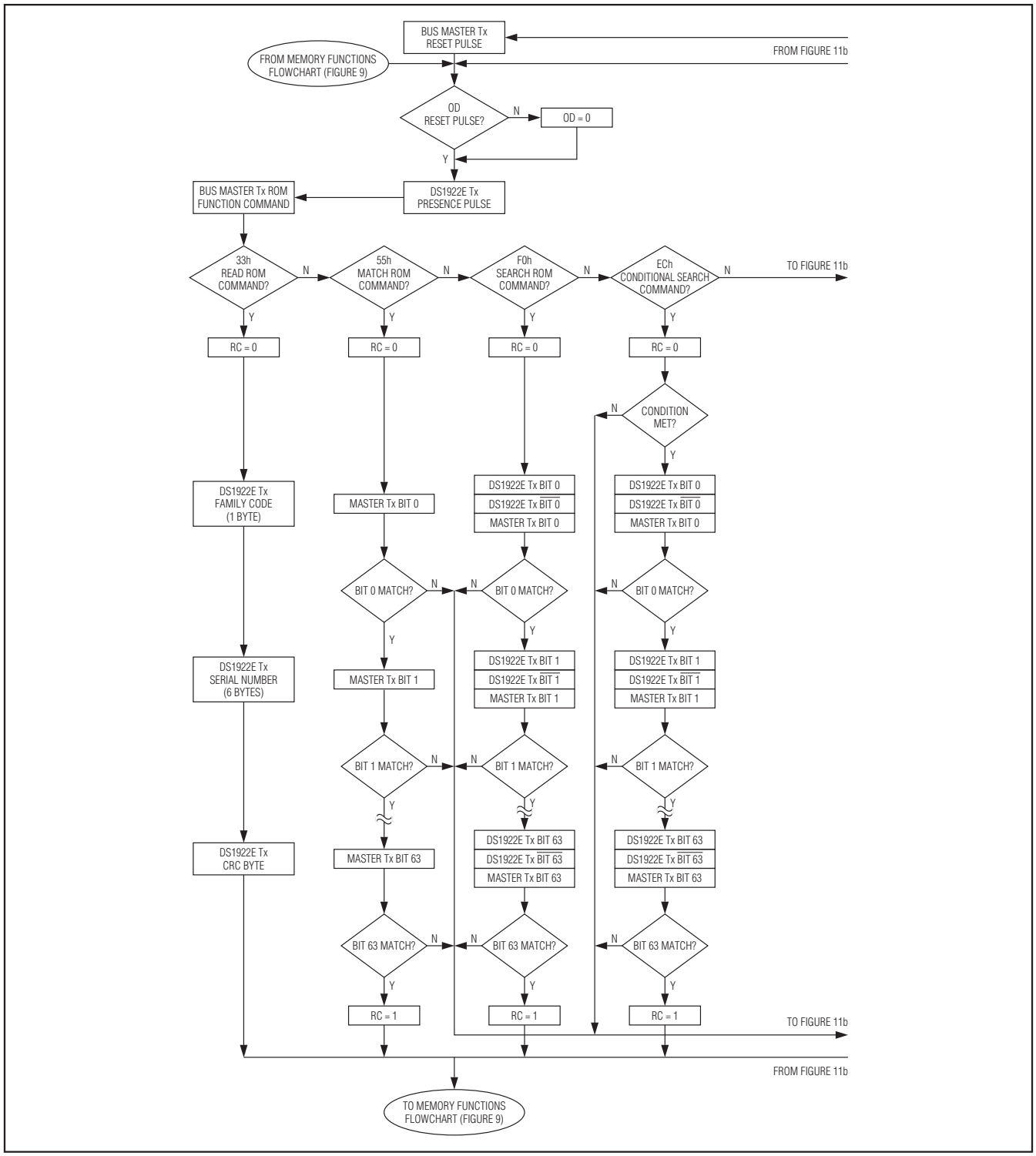


Figure 11a. ROM Functions Flowchart

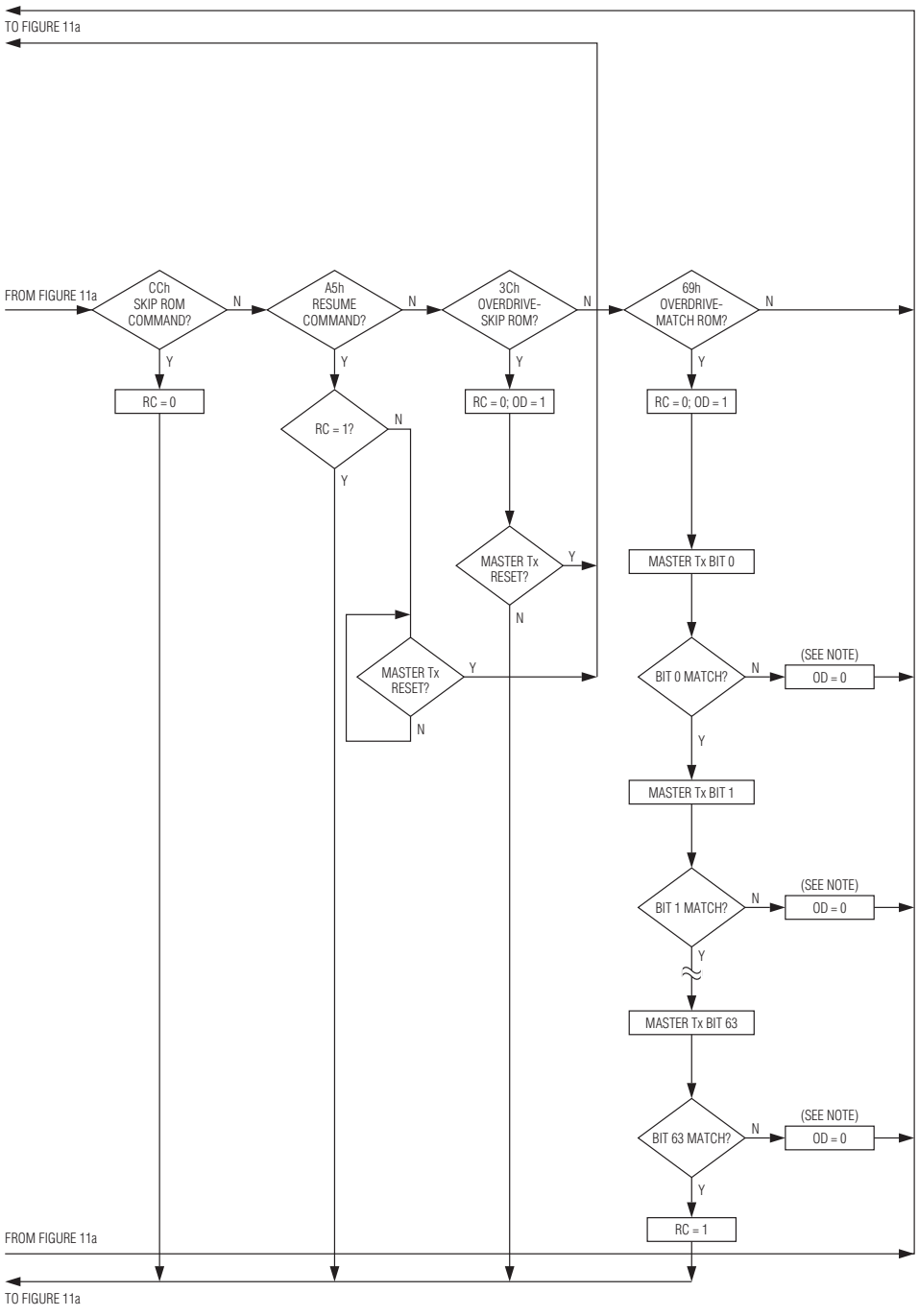


Figure 11b. ROM Functions Flowchart (continued)

1-Wire Signaling

The DS1922E requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus master initiates all these signals. The DS1922E can communicate at two different speeds: standard speed and overdrive speed. If not explicitly set into the Overdrive Mode, the DS1922E communicates at standard speed. While in Overdrive Mode the fast timing applies to all waveforms.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the threshold V_{TL}. To get from active to idle, the voltage needs to rise from V_{ILMAX} past the threshold V_{TH}. The time it takes for the voltage to make this rise is seen in Figure 12 as "ε" and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage V_{ILMAX} is relevant for the DS1922E when determining a logical level, not triggering any events.

The initialization sequence required to begin any communication with the DS1922E is shown in Figure 12. A reset pulse followed by a presence pulse indicates the DS1922E is ready to receive data, given the correct ROM and memory function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for t_{RSTL} + t_F to compensate for the edge. A t_{RSTL} duration of 690µs or longer exits the Overdrive Mode, returning the device to standard speed. If the DS1922E is in Overdrive Mode and t_{RSTL} is no longer than 80µs, the device remains in Overdrive Mode.

After the bus master has released the line, it goes into receive mode (Rx). Now the 1-Wire bus is pulled to V_{PUP} through the pullup resistor or, in the case of a DS2480B driver, through active circuitry. When the threshold V_{TH} is crossed, the DS1922E waits for t_{PDH} and then transmits a presence pulse by pulling the line low for t_{PDL}. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

The t_{RSTH} window must be at least the sum of t_{PDHMAX}, t_{PDLMAX}, and t_{RECMIN}. Immediately after t_{RSTH} is expired, the DS1922E is ready for data communication. In a mixed population network, t_{RSTH} should be extended to minimum 480µs at standard speed and 48µs at overdrive speed to accommodate other 1-Wire devices.

Read/Write Time Slots

Data communication with the DS1922E takes place in time slots that carry a single bit each. Write time slots transport data from bus master to slave. Read time slots transfer data from slave to master. The definitions of the write and read time slots are illustrated in Figure 13.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS1922E starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

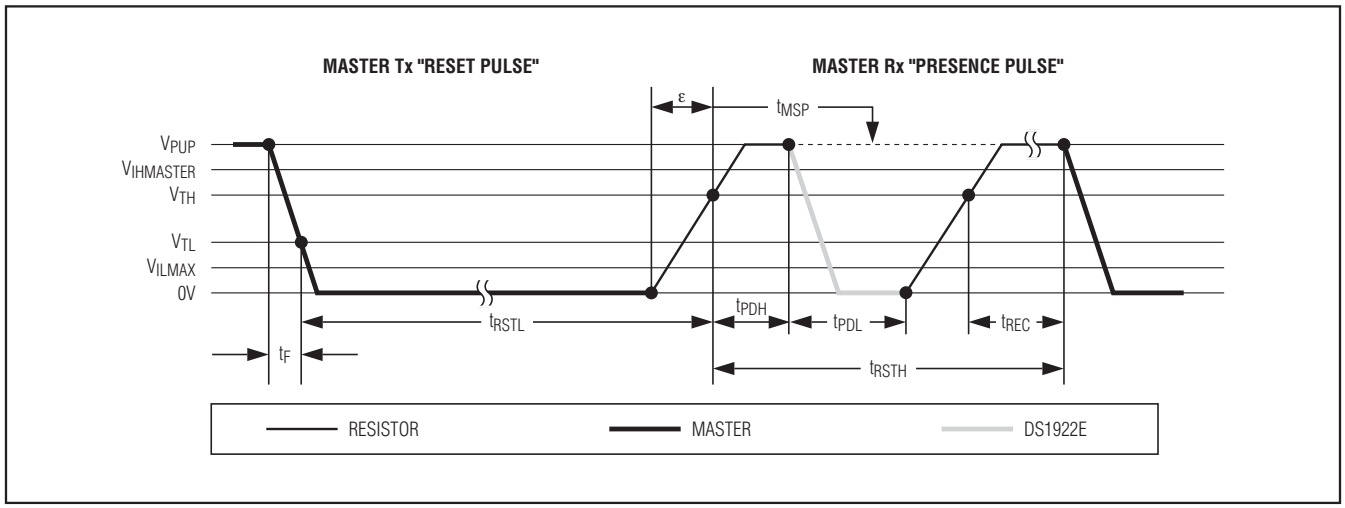


Figure 12. Initialization Procedure: Reset and Presence Pulse

Master-to-Slave

For a **write-one** time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time t_{W1LMAX} is expired. For a **write-zero** time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} is expired. The voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window. After the V_{TH} threshold has been crossed, the DS1922E needs a recovery time t_{REC} before it is ready for the next time slot.

Slave-to-Master

A **read-data** time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS1922E starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS1922E does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of $t_{RL} + \delta$ (rise time) on one side and the internal timing generator of the DS1922E on the other side define the master sampling window (t_{MSRMIN} to t_{MSRMAX}) in which the master must perform a read from the data line. For most reliable communication, t_{RL} should be as short as permissible and the master should read close to but no later than t_{MSRMAX}. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS1922E to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single DS1922E attached to a 1-Wire line. For multiple device configurations, t_{REC} must be extended to accommodate the additional 1-Wire device input capacitance. Alternatively, an interface that performs active pullup during the 1-Wire recovery time such as the DS2482-x00 or DS2480B 1-Wire line drivers can be used.

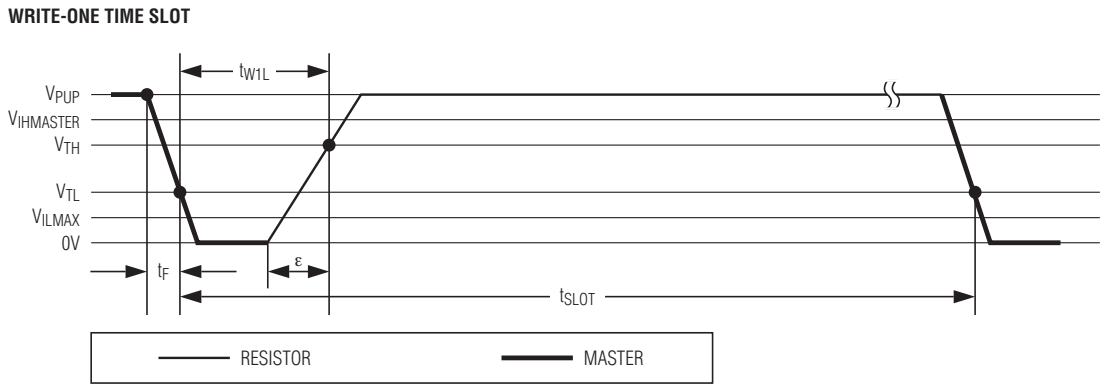
Improved Network Behavior (Switchpoint Hysteresis)

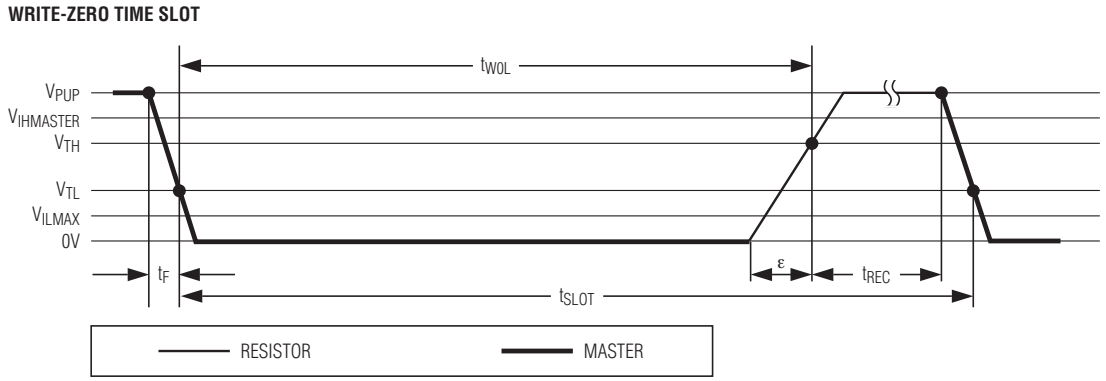
In a 1-Wire environment line termination is possible only during transients controlled by the bus master (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a slave device to lose synchronization with the master and, as a consequence, result in a Search ROM command coming to a dead end or cause a device-specific function command to abort. For better performance in network applications, the DS1922E uses a new 1-Wire front-end, which makes it less sensitive to noise and also reduces the magnitude of noise injected by the slave device itself.

The DS1922E's 1-Wire front-end differs from traditional slave devices in four characteristics:

1) The falling edge of the presence pulse has a controlled slew rate. This provides a better match to the line impedance than a digitally switched transistor, converting the high-frequency ringing known from traditional devices into a smoother low-bandwidth transition. The slew-rate control is specified by the parameter t_{FPD}, which has different values for standard and overdrive speed.
2) There is additional lowpass filtering in the circuit that detects the falling edge at the beginning of a time slot. This reduces the sensitivity to high-frequency noise. This additional filtering does not apply at overdrive speed.
3) There is a hysteresis at the low-to-high switching threshold V_{TH}. If a negative glitch crosses V_{TH} but does not go below $V_{TH} - V_{HY}$, it is not recognized (Figure 14, Case A). The hysteresis is effective at any 1-Wire speed.
4) There is a time window specified by the rising edge hold-off time t_{REH} during which glitches are ignored, even if they extend below $V_{TH} - V_{HY}$ threshold (Figure 14, Case B, $t_{GL} < t_{REH}$). Deep voltage droops or glitches that appear late after crossing the V_{TH} threshold and extend beyond the t_{REH} window cannot be filtered out and are taken as the beginning of a new time slot (Figure 14, Case C, $t_{GL} \geq t_{REH}$).

Devices that have the parameters t_{FPD}, V_{HY}, and t_{REH} specified in their electrical characteristics use the improved 1-Wire front-end.





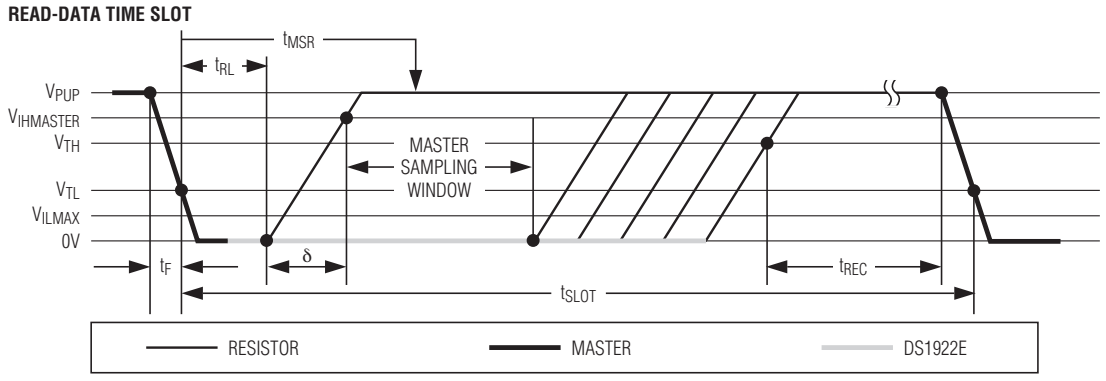


Figure 13. Read/Write Timing Diagrams

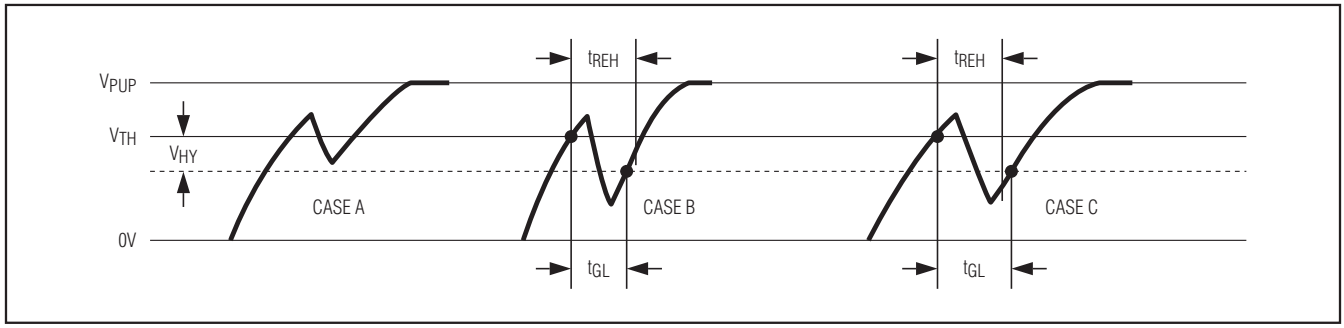


Figure 14. Noise Suppression Scheme

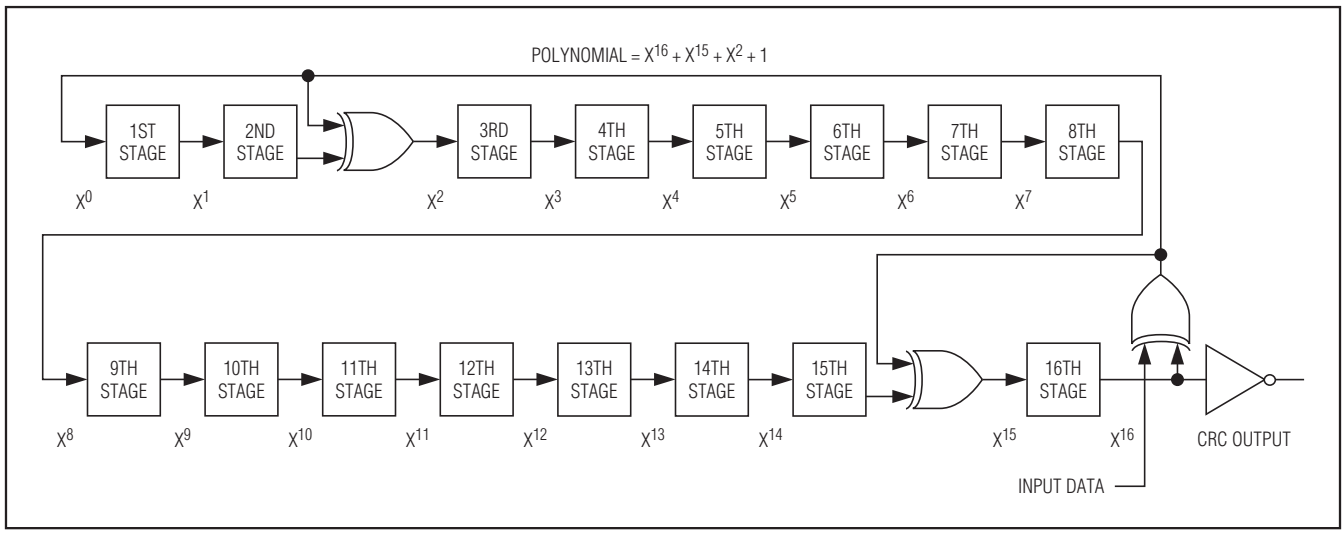


Figure 15. CRC-16 Hardware Description and Polynomial

CRC Generation

The DS1922E uses two types of CRCs. One CRC is an 8-bit type and is stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the DS1922E to determine if the ROM data has been received error-free. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. This 8-bit CRC is received in the true (noninverted) form, and it is computed at the factory and lasered into the ROM.

The other CRC is a 16-bit type, generated according to the standardized CRC-16 polynomial function $x^{16} + x^{15} + x^2 + 1$. This CRC is used for error detection when reading register pages or the data-log memory using the Read Memory with CRC command and for fast verification of a data transfer when writing to or reading from the scratchpad. In contrast to the 8-bit CRC, the 16-bit CRC is always communicated in the inverted form. A CRC generator inside the DS1922E (Figure 15) calculates a new 16-bit CRC as shown in the command flowchart of Figure 9. The bus master compares the CRC value read from the device to the one it calculates from the data and decides whether to continue with an operation or to reread the portion of the data with the CRC error. With the initial pass through the Read Memory with CRC flowchart, the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the two address bytes and the data bytes. The password is excluded from the CRC calculation. Subsequent passes through the Read Memory with CRC flowchart generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the data bytes.

With the Write Scratchpad command, the CRC is generated by first clearing the CRC generator and then shift-

ing in the command code, the target addresses TA1 and TA2, and all the data bytes. The DS1922E transmits this CRC only if the data bytes written to the scratchpad include scratchpad ending offset 11111b. The data can start at any location within the scratchpad.

With the Read Scratchpad command, the CRC is generated by first clearing the CRC generator and then shifting in the command code, the target addresses TA1 and TA2, the E/S byte, and the scratchpad data starting at the target address. The DS1922E transmits this CRC only if the reading continues through the end of the scratchpad, regardless of the actual ending offset. For more information on generating CRC values, refer to Application Note 27.

Command-Specific 1-Wire Communication Protocol—Legend

SYMBOL	DESCRIPTION
RST	1-Wire reset pulse generated by master.
PD	1-Wire presence pulse generated by slave.
Select	Command and data to satisfy the ROM function protocol.
WS	Command "Write Scratchpad."
RS	Command "Read Scratchpad."
CPS	Command "Copy Scratchpad with Password."
RMC	Command "Read Memory with Password and CRC."
CM	Command "Clear Memory with Password."
FC	Command "Forced Conversion."
SM	Command "Start Mission with Password."
STP	Command "Stop Mission with Password."
TA	Target Address TA1, TA2.
TA–E/S	Target Address TA1, TA2 with E/S byte.
<Data to EOS>	Transfer of as many data bytes as are needed to reach the scratchpad offset 1Fh.
<Data to EOP>	Transfer of as many data bytes as are needed to reach the end of a memory page.
<PW/Dummy>	Transfer of 8 bytes that either represent a valid password or acceptable dummy data.
<32 Bytes>	Transfer of 32 bytes.
<Data>	Transfer of an undetermined amount of data.
FFh	Transmission of one FFh byte.
$\overline{\text{CRC-16}}$	Transfer of an inverted CRC-16.
FF Loop	Indefinite loop where the master reads FF bytes.
AA Loop	Indefinite loop where the master reads AA bytes.
Busy	Interval during Copy Scratchpad where the DS1922E does not respond. Any bits read during this time are logic 1.

Command-Specific 1-Wire Communication Protocol—Color Codes

Master-to-Slave	Slave-to-Master

1-Wire Communication Examples

Write Scratchpad, Reaching the End of the Scratchpad (Cannot Fail)

RST	PD	Select	WS	TA	<Data to EOS>	$\overline{\text{CRC-16}}$	FF Loop

Read Scratchpad (Cannot Fail)

RST	PD	Select	RS	TA-E/S	<Data to EOS>	$\overline{\text{CRC-16}}$	FF Loop

Copy Scratchpad with Password (Success)

RST	PD	Select	CPS	TA-E/S	<PW/Dummy>	Busy	AA Loop

Copy Scratchpad with Password (Fail TA-E/S or Password)

RST	PD	Select	CPS	TA-E/S	<PW/Dummy>	FF Loop

Read Memory with Password and CRC (Success)

RST	PD	Select	RMC	TA	<PW/Dummy>	<Data to EOP>	$\overline{\text{CRC-16}}$

<32 Bytes>	$\overline{\text{CRC-16}}$	FF Loop

Loop

Read Memory with Password and CRC (Fail Password or Address)

RST	PD	Select	RMC	TA	<PW/Dummy>	FF Loop

Clear Memory with Password

RST	PD	Select	CM	<PW/Dummy>	FFh	FF Loop

To verify success, read the General Status register at address 0215h. If MEMCLR is 1, the command was executed successfully.

1-Wire Communication Examples (continued)

Forced Conversion

RST	PD	Select	FC	FFh	FF Loop

To read the result and to verify success, read the addresses 020Ch to 020Fh (results) and the device samples counter at address 0223h to 0225h. If the count has incremented, the command was executed successfully.

Start Mission with Password

RST	PD	Select	SM	<PW/Dummy>	FFh	FF Loop

To verify success, read the General Status register at address 0215h. If MIP is 1 and MEMCLR is 0, the command was executed successfully.

Stop Mission with Password

RST	PD	Select	STP	<PW/Dummy>	FFh	FF Loop

To verify success, read the General Status register at address 0215h. If MIP is 0, the command was executed successfully.

Mission Example: Prepare and Start a New Mission

Assumption: The previous mission has been ended by using the Stop Mission command. Passwords are not enabled.

Starting a mission requires three steps:

Step 1: Clear the data of the previous mission.

Step 2: Write the setup data to register page 1.

Step 3: Start the new mission.

Step 1: Clear the data of the previous mission.

With only a single device connected to the bus master, the communication of step 1 looks like this:

MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx	(Reset)	Reset pulse
Rx	(Presence)	Presence pulse
Tx	CCh	Issue “Skip ROM” command
Tx	96h	Issue “Clear Memory” command
Tx	<8 FFh bytes>	Send dummy password
Tx	FFh	Send dummy byte
Tx	(Reset)	Reset pulse
Rx	(Presence)	Presence pulse

Step 2: Write the setup data to register page 1.

During the setup, the device needs to learn the following information:

- Time and Date
- Sample Rate
- Alarm Thresholds
- Alarm Controls (Response to Conditional Search)
- General Mission Parameters (e.g., Channels to Log and Logging Format, Rollover, Start Mode)
- Mission Start Delay

The following data sets up the DS1922E for a mission that logs temperature using 8-bit format.

ADDRESS	DATA	EXAMPLE VALUES	FUNCTION
0200h	00h	15:30:00 hours	Time
0201h	30h		
0202h	15h		
0203h	01h	1st of April in 2008	Date
0204h	04h		
0205h	08h		
0206h	0Ah	Every 10 minutes (EHSS = 0)	Sample rate
0207h	00h		
0208h	08h	18°C low 135°C high	Temperature alarm thresholds
0209h	F2h		
020Ah	00h	(Don't care)	(Not applicable with DS1922E)
020Bh	FFh		
020Ch	FFh	(Don't care)	Clock through read-only registers
020Dh	FFh		
020Eh	FFh		
020Fh	FFh		
0210h	02h	Enable high alarm	Temperature alarm control
0211h	FCh	Disabled	(Not applicable with DS1922E)
0212h	01h	On (enabled), EHSS = 0 (low sample rate)	RTC oscillator control, sample rate selection
0213h	C1h	Normal start; no rollover; 8-bit temperature log	General mission control
0214h	FFh	(Don't care)	Clock through read-only registers
0215h	FFh		
0216h	5Ah	90 minutes	Mission start delay
0217h	00h		
0218h	00h		

With only a single device connected to the bus master, the communication of step 2 looks like this:

MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx	(Reset)	Reset pulse
Rx	(Presence)	Presence pulse
Tx	CCh	Issue “Skip ROM” command
Tx	0Fh	Issue “Write Scratchpad” command
Tx	00h	TA1, beginning offset = 00h
Tx	02h	TA2, address = 0200h
Tx	<25 Data Bytes>	Write 25 bytes of data to scratchpad
Tx	<7 FFh Bytes>	Write through the end of the scratchpad
Tx	(Reset)	Reset pulse
Rx	(Presence)	Presence pulse
Tx	CCh	Issue “Skip ROM” command
Tx	AAh	Issue “Read Scratchpad” command
Rx	00h	Read TA1, beginning offset = 00h
Rx	02h	Read TA2, address = 0200h
Rx	1Fh	Read E/S, ending offset = 1Fh, flags = 0h
Rx	<32 Data Bytes>	Read scratchpad data and verify
Tx	(Reset)	Reset pulse
Rx	(Presence)	Presence pulse
Tx	CCh	Issue “Skip ROM” command
Tx	99h	Issue “Copy Scratchpad” command
Tx	00h	TA1 (AUTHORIZATION CODE)
Tx	02h	TA2
Tx	1Fh	E/S
Tx	<8 FFh Bytes>	Send dummy password
Tx	(Reset)	Reset pulse
Rx	(Presence)	Presence pulse

Step 3: Start the new mission.

With only a single device connected to the bus master, the communication of step 3 looks like this:

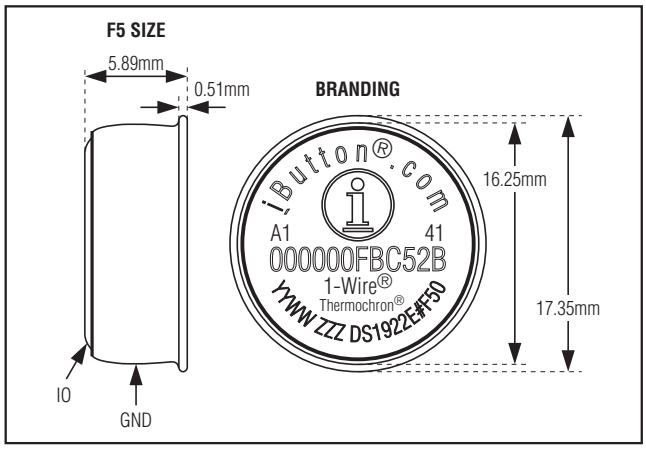
If step 3 was successful, the MIP bit in the General Status register is 1, the MEMCLR bit is 0, and the mission start delay counts down.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx	(Reset)	Reset pulse
Rx	(Presence)	Presence pulse
Tx	CCh	Issue “Skip ROM” command
Tx	CCh	Issue “Start Mission” command
Tx	<8 FFh Bytes>	Send dummy password
Tx	FFh	Send dummy byte
Tx	(Reset)	Reset pulse
Rx	(Presence)	Presence pulse

Software Correction Algorithm or Temperature

The correction algorithm described in the DS1922L/DS1922T data sheet does not apply to the DS1922E. If attempted, the corrected result is generally less accurate than the raw temperature data read from the device. Therefore, with the DS1922E the memory pages 18 and 19 are available as additional user memory.

Pin Configuration



Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
F5 Can	IB#6CB	21-0266	—

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/08	Initial release	—
1	10/08	Added the *Software Correction Algorithm for Temperature* section	43
2	6/09	Changed storage temperature range in *Absolute Maximum Ratings* and added a recommended storage temperature note for maximum battery lifetime	2
3	4/11	Updated UL certificate reference; added paragraph on validation certificates to *Detailed Description* section; added more details on the Device Samples Counter in the *Other Indicators* section	1, 5, 6, 18
4	6/13	Removed the UL 913 5th Ed. compliance statement from the *Common iButton Device Features* section and *iButton Can Physical Specification* table; reworded the *Electrical Characteristics* table Note 19	1, 4, 5
5	11/13	Added the Busy state during Copy Scratchpad to the *Command-Specific 1-Wire Communication Protocol—Legend* and *1-Wire Communication Examples* sections	38, 39
6	3/15	Updated *Benefits and Features* and *Common iButton Device Features* sections	1

